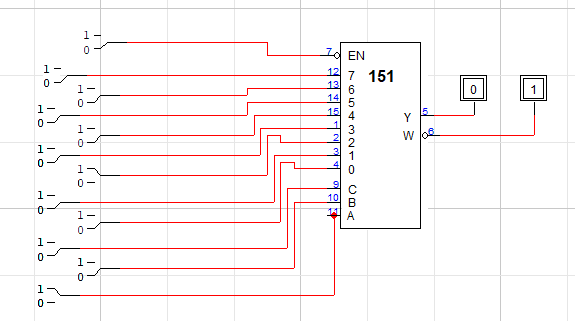
**DLD LAB 09**

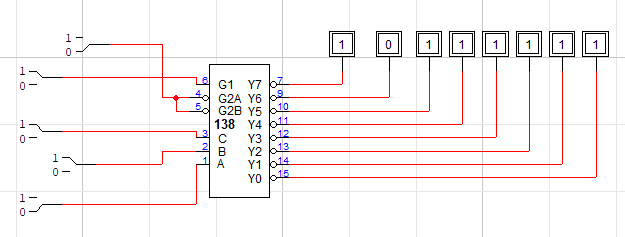
**Question 01**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **E’** | **S2** | **S1** | **S0** | **L0** | **L1** | **L2** | **L3** | **L4** | **L5** | **L6** | **L7** | **Z** | **Z’** |
| L | L | L | L | L | X | X | X | X | X | X | X | 0 | 1 |
| L | L | L | L | H | X | X | X | X | X | X | X | 1 | 0 |
| L | L | L | H | X | L | X | X | X | X | X | X | 0 | 1 |
| L | L | L | H | X | H | X | X | X | X | X | X | 1 | 0 |
| L | L | H | L | X | X | L | X | X | X | X | X | 0 | 1 |
| L | L | H | L | X | X | H | X | X | X | X | X | 1 | 0 |
| L | L | H | H | X | X | X | L | X | X | X | X | 0 | 1 |
| L | L | H | H | X | X | X | H | X | X | X | X | 1 | 0 |
| L | H | L | L | X | X | X | X | L | X | X | X | 0 | 1 |
| L | H | L | L | X | X | X | X | H | X | X | X | 1 | 0 |
| L | H | L | H | X | X | X | X | X | L | X | X | 0 | 1 |
| L | H | L | H | X | X | X | X | X | H | X | X | 1 | 0 |
| L | H | H | L | X | X | X | X | X | X | L | X | 0 | 1 |
| L | H | H | L | X | X | X | X | X | X | H | X | 1 | 0 |
| L | H | H | H | X | X | X | X | X | X | X | L | 0 | 1 |
| L | H | H | H | X | X | X | X | X | X | X | H | 1 | 0 |



**Question 02**

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **D** | **S0** | **S1** | **S2** | **l0** | **l1** | **L2** | **L3** | **L4** | **L5** | **L6** | **L7** |
| D | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| D | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| D | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| D | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| D | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| D | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| D | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| D | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |

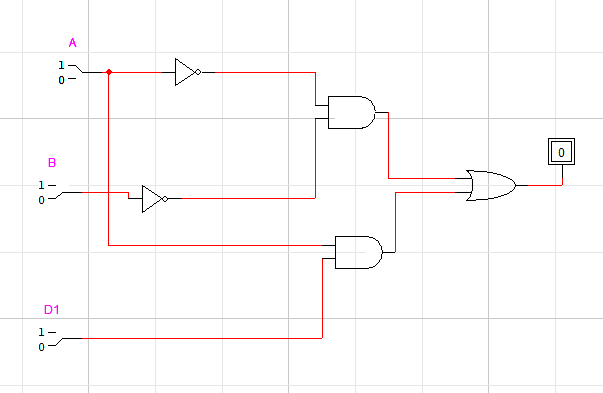


**Question 03**

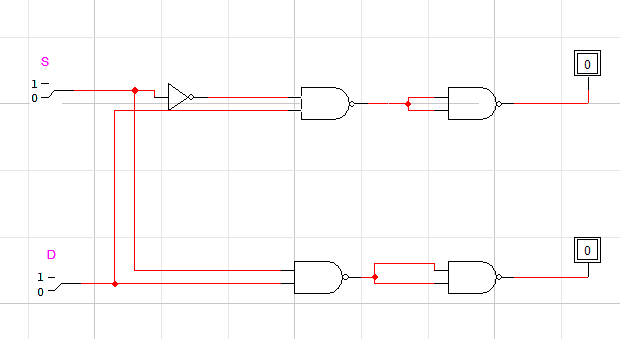
1. **Design NAND Logic Gate using 2:1 MUX**



1. **Design NOR Logic Gate using 2:1 MUX**



1. **Design 1:2 DEMUX using NAND Gate**



1. **Design 1:4 DEMUX using NAND Gate**

